REMARKS

Claims 1-23 are all the claims pending in the application. By this Amendment, Applicant amends claims 1 and 13-15 to further clarify the invention, and claim 17 for conformity therewith. In addition, Applicant rewrites claims 2, 10, and 18 into their independent forms. In order to provide more varied protection, Applicant adds claims 21-23, which are clearly supported throughout the specification.

I. Preliminary Matters

Applicant thanks the Examiner for returning the initialed form PTO/SB/08 submitted with the Information Disclosure Statement filed on December 19, 2005.

The Examiner has not indicated acceptance of the drawings filed on December 14, 2001. Applicant respectfully requests the Examiner to indicate acceptance of the drawing figures filed December 14, 2001.

II. Summary of the Office Action

The Examiner withdrew the previous rejections. The Examiner, however, found new grounds for rejecting the claims. Specifically, claims 1 and 5 are rejected under 35 U.S.C. § 112, second paragraph and claims 1, 5-8, 12-17, 19 and 20 are rejected under 35 U.S.C. § 103(a). Claims 2-4, 9-11, and 18 contain allowable subject matter.

III. Claim Rejections under 35 U.S.C. § 112

Claims 1-12 are rejected under 35 U.S.C. § 112, second paragraph, for minor informalities in claims 1 and 5. Applicant respectfully requests the Examiner to withdraw this rejection of claims 1-12 in view of the self-explanatory amendments being made herein to claim 1.

With respect to claim 5, Applicant respectfully traverses this rejection in view of the following comments. The Examiner alleges that there are insufficient antecedent basis for the term "the respective selected" recited in claim 5 (*see* page 2 of the Office Action). Applicant respectfully disagrees. Applicant respectfully submits that claim 5 recites: "selection means for selecting one of the at least one first delayed clock signal and the second delayed clock signal and, optionally, one of the at least one first clock signal and the second clock signal." The selection means selecting at least one of... provides the antecedent basis for the "respective selected" one of.... Accordingly, Applicant respectfully requests the Examiner to withdraw this rejection of claim 5.

IV. Claim Rejections under 35 U.S.C. § 103

Claims 1, 5-8, 12-17 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,455,840 to Nakauchi et al. (hereinafter "Nakauchi") in view of U.S. Patent No, 6,845,457 to Mirov et al. (hereinafter "Mirov"). Applicant respectfully traverses these grounds for rejection in view of the following comments.

In general, the present invention relates to redundant internal clock generators because for purpose of internal redundancy, phase hits are not tolerated. In general, synchronous telecommunication equipment such as a digital cross-connect may have two redundant internal clock generators, which are typically both synchronized on the same external reference clock. Since such systems are of modular design, the modules need to be interconnected by internal cabling (electrical or optical).

In particular, each module (for example a matrix stage) must be supplied by both redundant clock generators to fully protect the function of the equipment. In this case, it is

necessary that the two redundant clock signals, as these are received at the respective module, are phase aligned. In the conventional techniques, the use of matched cables of exactly the same length was required so that cable delay was the same for both redundant clock signals. In a preferred embodiment of the present invention, however, this situation is improved by providing a fixed delay for the first clock signal. This fixed delay corresponds to the maximum allowable cable delay/length (*e.g.* 400 m). The second clock signal is delayed by a variable delay that corresponds to twice the maximum cable delay. This way, all possible cabling situations can be compensated for by using only one adjustable delay element and corresponding control instance. In other words, two delayed clock signals are phase adjusted to each other.

Nakauchi relates to a method of compensating a phase of a system clock for use in a system clock circuit for receiving an external clock to produce a system clock for an information processing system, in which the quantity of phase variation of the external clock supplied from a reference clock oscillator provided outside the system is detected. In accordance with the detected quantity of phase variation, the phase variation of the external clock supplied from the reference clock generator is compensated to supply the compensated external clock to the system clock circuit (*see* Abstract and col. 3, lines 33 to 45).

Specifically, Nakauchi discloses a system clock generating circuit that includes a frequency synthesizer or a system clock circuit PLL 31, a circuit 40 for compensating a phase of a system clock, a circuit 41 for detecting an abnormality of an external clock, a delay circuit 42 and a selector 43. The output clock of the PLL 31 is supplied as a system clock to an information processing system 100 (Fig. 3). In Nakauchi, the external clock is input into PLL 31 unless an abnormality is detected. When the abnormality is detected, the output clock 46 of the

phase compensating circuit is used as the PLL input clock 44 (instead of directly using the external clock 26). Therefore, unstable retracting operations are prevented (Fig. 3; col. 5, line 44 to col. 6, line 59).

Mirov relates to a method for controlling transitions between a first and second clock frequency signal in first and second components electrically coupled together and in communication with one another. The method includes asserting a freeze signal to cause communications between the first and second components to cease. A freeze acknowledge signal is then received from the first and second components, indicating that communications therebetween have ceased. A change signal is delivered to the first and second components to cause the components to switch between the first and second clock frequency signals (*see* Abstract and col. 2, lines 19 to 45).

Specifically, Mirov discloses a phased lock loop (PLL) controller 500 having a first divide-by-N counter 502 that receives the Clock A signal 410 and produces a desired, reduced-frequency clock signal, which is delivered to an input terminal of a conventional phase comparator 504. An output terminal of the phase comparator 504 is coupled to a conventional voltage controlled oscillator (VCO) 506 through a loop filter 505. A second divide-by-N counter 508 is coupled to an output terminal of the VCO 506. An output terminal of the second divide-by-N counter 508 is coupled to a conventional clock tree 510, which may produce a plurality of clock signals, including the Clock B signal 412. The Clock B signal is coupled through a delay circuit 512 to a second input of the phase comparator 504. In Mirov, the Clock A signal 410 is at a preselected frequency, the Clock B signal 412 will be at the same frequency as the Clock A signal and is synchronized with the Clock A signal 410. The Clock A signal 410 is principally

unchanged, with the exception of a short delay D1. The clock tree 510 receives the delayed signal and produces the Clock B signal 412. A feedback path through the delay circuit 512 delivers the Clock B signal to the second input of the phase comparator 504. Any difference between the phases of the delayed Clock B signal 412 and the delayed Clock A signal 410 causes the phase comparator to deliver an output signal that varies the phase of the VCO 506. This process continues until the Clock B signal 412 is synchronized with the Clock A signal 410 (Fig. 5; col. 9, line 18 to col. 10, line 25).

The Examiner alleges that one of ordinary skill in the art would have been motivated to combine the references to further minimize the latency of the received data (*see* page 4 of the Office Action). Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of combinability, in whatever form, must nevertheless be "**clear and particular**." *Winner International Royalty Corporation v. Ching-Rong Wang*, 53 USPQ2d 1580, 1586-87 (Fed. Cir. 2000). It is respectfully submitted that the Examiner's rationale for combining the references is not understood. At the very least it is unclear how combining Mirov with Nakauchi would reduce the latency of received data.

Moreover, one of ordinary skill in the art would not have been motivated to combine the references. Nakauchi already discloses delaying the external clock signal and compensating for the phase difference when the external clock signal is abnormal. Mirov deals with controlling transitions between the clock frequencies. In Mirov, the controller adjusts the generated clock signal until it is synchronized with the external clock signal. If the system of Nakauchi would have been modified to include the system of Mirov, it would significantly change the principle operation of Nakauchi's system. That is, instead of selecting the external clock signal or the

clock signal 46, as disclosed in Nakauchi, the system would have been modifying the clock signal 46 until it is adjusted to the external clock. However, if the external clock signal is faulty, this modification would defeat the whole purpose of Nakauchi's system. In short, one of ordinary skill in the art would not have and could not have combined the references in the manner suggested by the Examiner.

Furthermore, the combined disclosure of Nakauchi and Mirov does not disclose or suggest "adjusting means for the phase adjustment of the second delay means, so that the delayed second clock signal is adapted to the phase of the delayed first clock signal at an output end of the first delay means, wherein the first clock signal and the second clock signal are internally generated within a network device," as set forth in claim 1.

That is, Nakauchi only discloses detecting abnormality in an external clock signal and using an adjusted external clock signal when such abnormality is detected. Mirov, on the other hand, discloses adjusting an internal clock signal to the external clock signal. In other words, both references fail to disclose or suggest having two internal signals, which are both delayed and where the second delayed internal signal is adjusted to the phase of the first delayed internal clock signal. In short, both references fail to disclose or suggest internal synchronization, in which two internal clock signals are adjusted.

For at least these exemplary reasons, claim 1 is patentable over Nakauchi and Mirov, while lack synchronization of two internal clock signals. Accordingly, it is appropriate and necessary for the Examiner to withdraw this rejection of claim 1. Claims 5-8, 13, 16, 17, 19, and 20 are patentable at least by virtue of their dependency on claim 1. Independent claims 13 and 14 recite features similar to, although not necessarily coextensive with, the features argued above

with respect to claim 1 and are patentable for at least analogous reasons. Accordingly, it is appropriate and necessary for the Examiner to withdraw this rejection of claims 13 and 14.

Independent claim 15, among a number of unique features, recites: "modifying by the compensation module the second delay time such that the delayed second clock signal is adapted to the phase of the delayed, at least one first clock signal." The combined disclosure of Nakauchi and Mirov fail to disclose or suggest a relationship between the delay time. That is, as acknowledged by the Examiner (*see* pages 3-4 of the Office Action), Nakauchi does not disclose or suggest modifying the second delay time. Mirov does not cure the deficient disclosure of Nakauchi in that it does not disclose or suggest modifying the delay time. Mirov only discloses modifying the generated clock signal B and not the delay time. Accordingly, the combined disclosure of Nakauchi and Mirov fails to disclose or suggest the unique features of claim 15. It is appropriate and necessary for the Examiner to withdraw this rejection of claim 15.

V. Allowable Subject Matter

Claims 2-4, 9-11, and 18 contain allowable subject matter. Claims 2, 10, and 18 have been rewritten into their independent form. Accordingly, it is appropriate and necessary for the Examiner to now allow claims 2, 10, and 18.

Applicant respectfully holds in abeyance the rewriting of claims 3, 4, 9, and 11 until arguments presented with respect to claim 1 have been reconsidered.

Applicant does not acquiesce to the Examiner's reasons for allowance.

VI. New Claims

In order to provide more varied protection, Applicant adds claims 21-23, which are patentable at least by virtue of their dependency on claim 14 or 15.

VII. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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